CLAIMS

1. An assertion generating system that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit, comprising:

a specification inputting unit that generates design data or specifications and a document for confirming a specification of the semiconductor integrated circuit by graphically editing the specification of the semiconductor integrated circuit based on user operations;

a first storing unit that stores the design data generated by the specification inputting unit;

a property generating unit that generates a property which verifies the specification of the semiconductor integrated circuit by reading the design data generated by the specification inputting unit from the first storing unit and using the read design data;

a second storing unit that stores the property generated by the property generating unit; and

an assertion generating unit that converts the property into an assertion description by reading the property generated by the property generating unit from the second storing unit, wherein

the property generated by the property generating

unit is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

2. The assertion generating system as claimed in claim 1, wherein

the property generating unit generates at least one or more properties, and

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

3. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

4. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit includes a design data generating unit that generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

5. The assertion generating system as claimed in claim 4, wherein

the assertion generating unit converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited by the specification inputting unit is added, and the property is the temporal property.

6. The assertion generating system as claimed in claim 1, wherein

the specification inputting unit is a business tool of spread sheet software and expands the design data into a graphic structure and inputs the graphic structure in the first storing unit.

7. A program that makes a computer function as the units of the assertion generating system as claimed in claim 1.

8. A circuit verifying system, comprising:

the assertion generating system as claimed in claim1, wherein

the circuit verifying system executes assertion verification of a semiconductor integrated circuit by using the assertion description generated by the assertion generating system.

9. An assertion generating method that generates an assertion description which is used for assertion verification of a semiconductor integrated circuit by a computer which has a program, comprising:

a specification inputting step that generates design data of the semiconductor integrated circuit by graphically editing a specification of the semiconductor integrated circuit based on user operations and inputs the design data in storage;

a property generating step that reads the design data generated at the specification inputting step from the storage and generates a property which verifies the

specification of the semiconductor integrated circuit using the read design data and inputs the property in the storage; and

an assertion generating step that reads the property generated at the property generating step from the storage and converts the property into an assertion description, wherein

the property generated by the property generating step is a selection condition with respect to a state transition, a logic value of at least one or more signals, or at least one or more signals in the design data.

10. The assertion generating method as claimed in claim 9, wherein

the property generating step generates at least one or more properties, and

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a state transition table or a state transition figure based on user operations.

11. The assertion generating method as claimed in claim 9, wherein

the specification inputting step generates the

design data of the semiconductor integrated circuit by editing a process sequence of the semiconductor integrated circuit into a timing chart or a time series figure based on user operations, and the property is a sequence property.

12. The assertion generating method as claimed in claim 9, wherein

the specification inputting step generates the design data of the semiconductor integrated circuit by editing the specification of the semiconductor integrated circuit with the use of a logic table or a state table based on user operations, and the property is a temporal property.

13. The assertion generating method as claimed in claim 12, wherein

the assertion generating step converts the property into an assertion description in which an assertion name composed of a table name or a table row number of the logic table or the state table, or a signal name or a state name in the logic table or the state table edited at the specification inputting step is added, and the property is the temporal property.

14. The assertion generating method as claimed in claim 9, wherein

the specification inputting step expands the design data into a graphic structure and inputs the graphic structure in the storage.

15. A manufacturing method of a semiconductor device, comprising:

a designing step that designs an integrated circuit having a predetermined function;

a simulating step that simulates the integrated circuit by using the assertion generated at the assertion generating method as claimed in claim 9; and

a manufacturing step that manufactures a semiconductor device based on specifications of the integrated circuit,

wherein

the semiconductor device in which design meeting specifications is confirmed is manufactured by that the integrated circuit is simulated by the assertion obtained at the assertion generating method as claimed in claim 9.